Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method comprising:

causing a device including a plurality of memory cells asymmetric transition times between at least two states to be programmed by

in a fast write mode, exclusively transitioning a plurality of said memory cells from a first state having a longer transition time to achieve to a second state having a shorter transition time to achieve, and

in a normal write mode, overwriting a plurality of memory cells, said overwriting comprising transitioning a plurality of said memory cells in the first state to the second state and transitioning another plurality of said memory cells in the second state to the first state,

wherein said transitioning comprises heating each of said memory cells by activating an electrically addressable transistor in a memory cell.

2. (Canceled)

3. (Original) The method of claim 1, wherein each memory cell includes a phase change material.

4. (Original) The method of claim 3, wherein the phase change material comprises a chalcogenide alloy.

5-7. (Canceled).

8. (Original) The method of claim 1, further comprising:

determining if the device has been written to; and

setting an indicator to a used status in response to determining that the device has been written to.

9. (Currently amended) A method comprising:

setting a plurality of memory cells in one of a plurality of zones of a memory device with asymmetric transition times between at least two states to a first state having a transition time to achieve; and

in a fast write mode, exclusively programming memory cells in the one or more zones by exclusively transitioning cells from the first state to a second state having a shorter transition time to achieve; and

in a normal write mode, overwriting a plurality of memory cells outside of said one or more zones, said overwriting comprising transitioning a plurality of said memory cells in the first state to the second state and transitioning another plurality of said memory cells in the second state to the first state,

wherein said transitioning comprises heating each of said memory cells by activating an electrically addressable transistor in a memory cell.

10. (Original) The method of claim 9, further comprising:

receiving a command to set memory cells in the zone to the first state; and

setting said memory cells to the first state.

11. (Original) The method of claim 9, further comprising setting the memory cells to the first state after a first use of the device.

12. (Original) The method of claim 10, further comprising:

receiving an indication that the memory device is preparing to initiate a data download; and

setting said plurality of memory cells in the zone to the first state.

13. (Currently amended) An apparatus comprising:

a writer unit operative to write data to a memory device having an asymmetric transition time between two memory states, wherein a transition from a first memory state to a second memory state takes longer than a transition from the second memory state to the first memory state, the writer unit comprising a controller operative to selectively control electrically transistors in said plurality of memory cells to heat each of said plurality of memory cells; and

a controller operative to

in a fast write mode, control the write unit to write exclusively to memory cells to be transitioned to the first memory state, and

in a normal write mode, overwrite a plurality of memory cells, said overwriting comprising transitioning a plurality of said memory cells in the first state to the second state and transitioning another plurality of said memory cells in the second state to the first state.

14. (Original) The apparatus of claim 13, wherein the apparatus comprises a non-volatile phase change memory device.

15. (Previously Presented) The apparatus of claim 13, further comprising a reader unit operative to determine if a use of the memory device is a first use, wherein the controller is operative to control the write unit to write exclusively to memory cells to be transitioned to the first memory state in response to determining that the use is the first use.

16. (Original) The apparatus of claim 13, wherein the controller is operative to control the write unit to reset a plurality of memory cells in a zone to the second memory state.

17. (Original) The apparatus of claim 16, wherein the controller is operative to control the write unit to write exclusively to memory cells in the zone.

18-21. (Canceled).

22. (Currently amended) An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

set a plurality of memory cells in one of a plurality of zones of a memory device with asymmetric transition times between at least two states to a first state having a transition time to achieve; and

in a fast write mode, exclusively program memory cells in the one or more zones by exclusively transitioning cells from the first state to a second state having a shorter transition time to achieve; and

in a normal write mode, overwrite a plurality of memory cells outside of said one or more zones, said overwriting comprising transitioning a plurality of said memory cells in the first state to the second state and transitioning another plurality of said memory cells in the second state to the first state,

wherein said transitioning comprises heating each of said memory cells by activating an electrically addressable transistor in a memory cell.

23. (Original) The article of claim 22, further comprising instructions operative to cause the machine to:

receive a command to set memory cells in the zone to the first state; and

set said memory cells to the first state.

24. (New) A method comprising:

causing a device including a plurality of memory cells, each including a phase change material, to be programmed with asymmetric transition times between at least two states by

exclusively transitioning a plurality of said cells from a first state having a longer transition time to achieve to a second state having a shorter transition time to achieve,

wherein said transitioning comprises heating each of said memory cells by activating a circuit to selectively provide electrical energy to at least one of said memory cells.